DRAFT

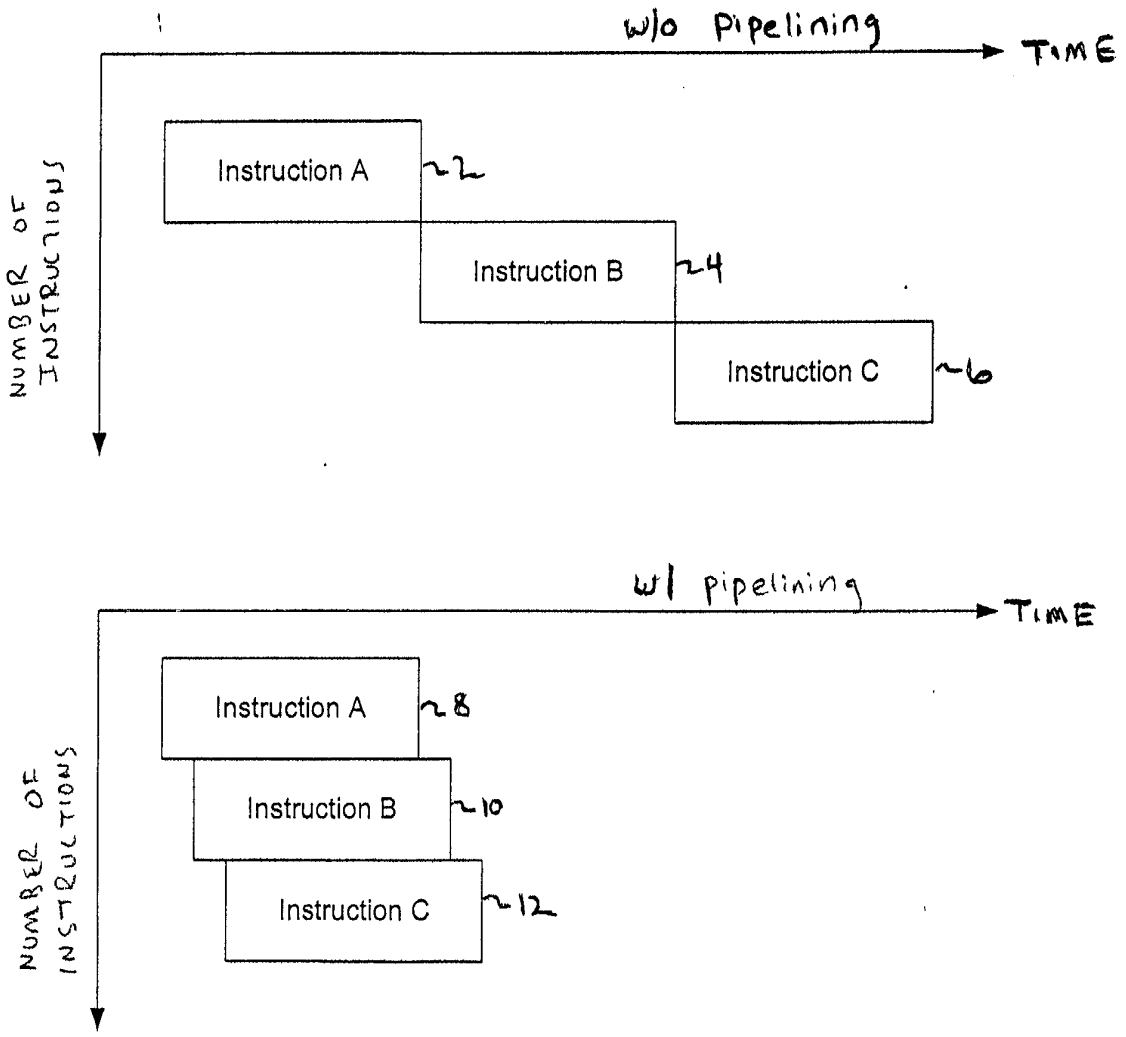

FIGURE 1 (PRIOR ART)

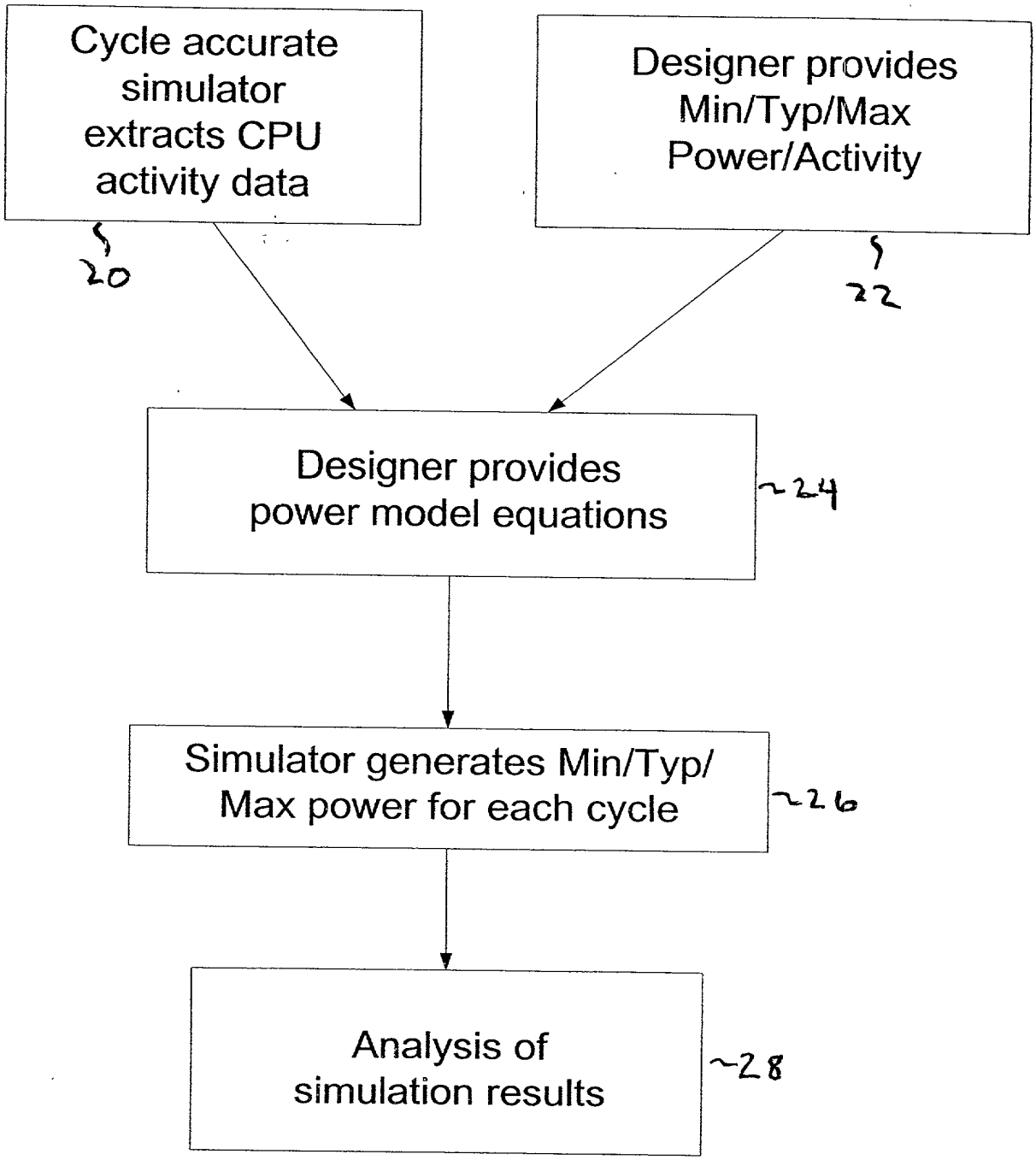

Figure 2 (Prior art)

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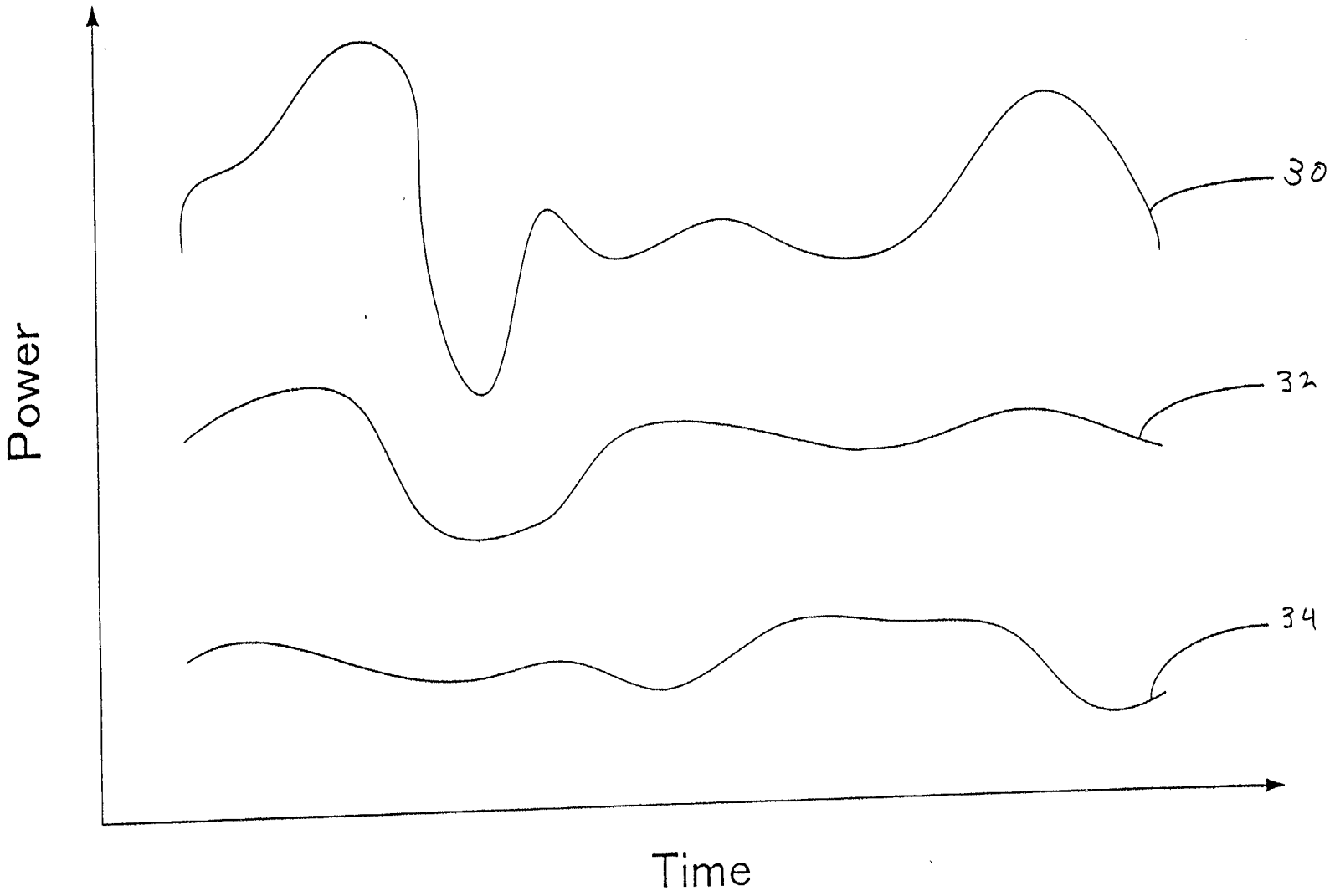

Figure 3 (Prior Art)

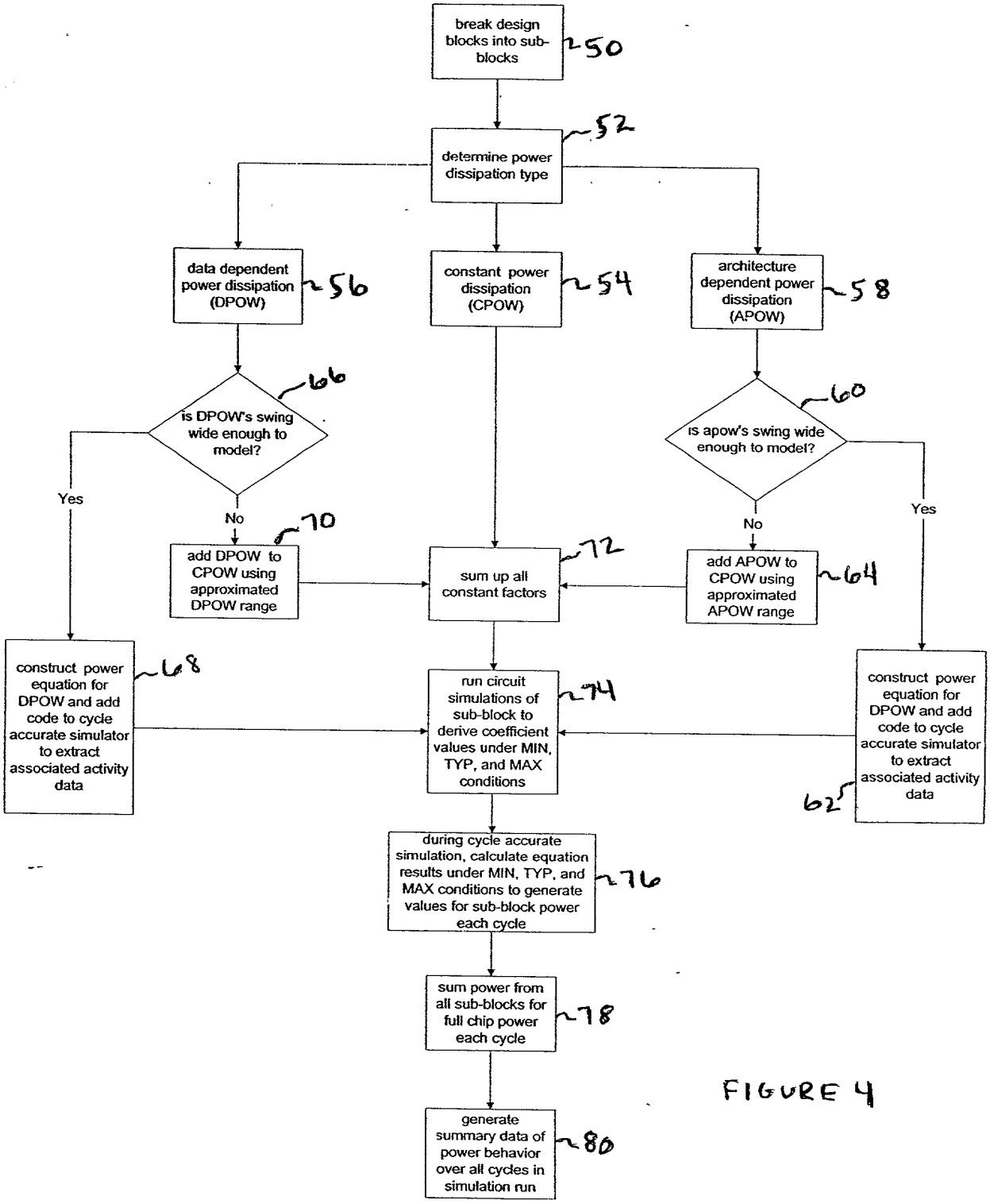
break design blocks into sub-blocks
50
determine power dissipation type
52
data dependent power dissipation (DPOW)
56
constant power dissipation (CPOW)
54
architecture dependent power dissipation (APOW)
58
is DPOW's swing wide enough to model?
66
Yes
No
70
add DPOW to CPOW using approximated DPOW range
is apow's swing wide enough to model?
60
No
Yes
add APOW to CPOW using approximated APOW range
64
sum up all constant factors
72
construct power equation for DPOW and add code to cycle accurate simulator to extract associated activity data
68
run circuit simulations of sub-block to derive coefficient values under MIN, TYP, and MAX conditions
74
construct power equation for DPOW and add code to cycle accurate simulator to extract associated activity data
62
during cycle accurate simulation, calculate equation results under MIN, TYP, and MAX conditions to generate values for sub-block power each cycle
76
sum power from all sub-blocks for full chip power each cycle
78
generate summary data of power behavior over all cycles in simulation run
80

FIGURE 4